



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,882	12/29/2000	Gralf Gaedeken	450117-02963	8380
20999	7590	04/07/2006		
FROMMER LAWRENCE & HAUG 745 FIFTH AVENUE- 10TH FL. NEW YORK, NY 10151			EXAMINER JONES, PRENELL P	
			ART UNIT 2616	PAPER NUMBER

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/751,882

Applicant(s)

GAEDEKEN ET AL.

Examiner

Prenell P. Jones

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 97-123 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 113-123 is/are allowed.
- 6) ☐ Claim(s) 97-101, 104-112 is/are rejected.
- 7) ☐ Claim(s) 102 and 103 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Arguments

1. Applicant's arguments with respect to claims 97- 123 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 101, 107, 109-112 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 101, in line 2, "assigns an ***appropriate*** channel number", which is vague.

Regarding claim 107, in line 3-4, Applicant is claiming "***predetermined other destination, which is the only further destination*** on respective data bus connected to said other destination", which is not clear to Examiner as to exactly what Applicant is claiming.

Regarding claim 109, on page 6, line 7-8, Applicant is claiming "***channel numbers of a data channels which will be accepted that carry data packets***", which is unclear to Examiner as to what exactly Applicant is claiming.

Claim Objections

4. Claim 106 is objected to because of the following informalities: In line 4, Applicant is claiming "saidsecond", which appears to be a typographical error. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 97-99, 100, 104-106, 108-111 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al (US PAT 6,751,221) in view of Moshier (US PAT 4,228,498).

Regarding claims 97-99, 104-106, 108 and 109, Saito discloses interfacing a first data bus to a data interface (Fig. 3, ATM, guide server, switch router/ATM network/NIU/1394

Art Unit: 2616

bus/gateway or bridge and video terminal consist of physical ports/portal (interface link layer) directly/indirectly interfacing between various nodes/devices, which are FANP nodes/device, wherein first 1394 bus 112 has a physical port that interconnects NIU/interface and gateway/bridge, col. 28, line 30-35), a plurality of additional 1394 buses are utilized along with associated registers (Figs. 10-14), uplink means (Fig. 30, upstream nodes (FANP nodes, such as gateway 105) recognized downstream node (NIU) transmitting data via 1394 bus on the uplink, col. 30, line 8-65, col. 40, line 9-35) configured and adapted for receiving data packets from the data bus (Fig. 3, 1394 gateway 105 recognize that data has come from the NIU of the first bus 112, therefore the NIU transmits data to gateway 105, whereby the data has to travel (be received by 1394 port) to the first 1394 bus 112 via a physical port in order to get to gateway 105, col. 30, line 8-65) each of the data packet is associated with one of a plurality of channels (Fig. 31, plurality of VCs/ plurality channels between guide server and cell router) determining the channel with which each data packet is associated with (Fig. 31, physical port of router and physical port of 1394 bus is associated with ATM network as to determine the VC for transmitting packet, packet is recognized and allowed to pass via VC routing table for transferring data, determining for each packet its respective VC channel, col. 24, line 38-51, line 64-67, col. 25, line 7-36, col. 26, line 22-46, col. 28, line 8-57), predetermined destination or channel number associated with the communication from a first bus to a second bus, multiple registers associated with destination identifiers, wherein destination address or channel number is associated with a specific register (col. 27, line 40-61, col. 28, line 36-57, predetermined destination). Saito is silent on a bus enable register identifying additional bus that serves a predetermined destination, in a communication system wherein the architecture utilizes multiple buses to increase execution speed, Moshier discloses in a computing process a bus enable register that monitors bit configuration, bus enable register is coupled to a bus address register

that is associated with destination address (Fig. col. 7, line 28-45, col. 8, line 28-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement bus enable registers identifying an additional bus and associated predetermined destination as taught by Moshier with the teachings of Saito for the purpose of identifying input source with respect to making data available for processing.

Regarding claim 100, 110 and 111, as indicated above, Saito discloses interfacing a first data bus to a data interface (Fig. 3, ATM, guide server, switch router/ATM network/NIU/1394 bus/gateway or bridge and video terminal consist of physical ports/portal (interface link layer) directly/indirectly interfacing between various nodes/devices, which are FANP nodes/device, wherein first 1394 bus 112 has a physical port that interconnects NIU/interface and gateway/bridge, col. 28, line 30-35), a plurality of additional 1394 buses are utilized along with associated registers (Figs. 10-14), uplink means (Fig. 30, upstream nodes (FANP nodes, such as gateway 105) recognized downstream node (NIU) transmitting data via 1394 bus on the uplink, col. 30, line 8-65, col. 40, line 9-35) configured and adapted for receiving data packets from the data bus (Fig. 3, 1394 gateway 105 recognize that data has come from the NIU of the first bus 112, therefore the NIU transmits data to gateway 105, whereby the data has to travel (be received by 1394 port) to the first 1394 bus 112 via a physical port in order to get to gateway 105, col. 30, line 8-65) each of the data packet is associated with one of a plurality of channels, Saito further discloses register storing source node and destination node identifiers, and available bandwidth (col. 69, line 1-67).

Art Unit: 2616

Regarding claim 104, Saito further discloses a switch control unit (controllable switch) that has function for processing IP packet or FANP between interface ports/interface link layer and associated buses (Fig. 6, col. 25, line 3-67).

4. Claim 112 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al (US PAT 6,751,221) in view of Moshier (US PAT 4,228,498) as applied to claims above, and further in view of Cannella (US PAT 668,810).

Regarding claim 112, as indicated above, Saito discloses interfacing a first data bus to a data interface (Fig. 3, ATM, guide server, switch router/ATM network/NIU/1394 bus/gateway or bridge and video terminal consist of physical ports/portal (interface link layer) directly/indirectly interfacing between various nodes/devices, which are FANP nodes/device, wherein first 1394 bus 112 has a physical port that interconnects NIU/interface and gateway/bridge, col. 28, line 30-35), a plurality of additional 1394 buses are utilized along with associated registers, and Moshier discloses in a computing process a bus enable register that monitors bit configuration, bus enable register is coupled to a bus address register that is associated with destination address (Fig. col. 7, line 28-45, col. 8, line 28-45). However, both Saito and Moshier are silent on storing payload in register. In a data communication environment, Cannella discloses interface link layer for bit synchronization wherein bit count and payload are stored in register. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement storing payload in a register associated with interface link layer as taught by Cannella with the combined teachings of Saito and Moshier for the purpose of further aiding in the making data available for processing.

Allowable Subject Matter

5. Claims 113-123 allowed over prior art.
6. Claims 102 and 103 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Although the combined prior art disclose interfacing a first data bus to a data interface (ports/interface link layer), directly/indirectly interfacing between various nodes/devices, which are FANP nodes/device, wherein a plurality of 1394 buses are utilizes wherein there is a first bus and a plurality of additional 1394 buses are utilized along with associated registers, uplink means/upstream nodes (FANP nodes, such as gateway 105) recognized downstream node (NIU) transmitting data via 1394 bus on the uplink configured and adapted for receiving data packets from the data bus, each of the data packet is associated with one of a plurality of channels, determining the channel with which each data packet is associated with, predetermined destination or channel number associated with the communication from a first bus to a second bus, multiple registers associated with destination identifiers, wherein destination address or channel number is associated with a specific register, a computing process a bus enable register that monitors bit configuration, bus enable register is coupled to a bus address register that is associated with destination address, they fail to teach or suggest with respect to claim 102, uplink comprise packetizer able to repack data packets received from the first data bus into a format of the transmission path that is different to the format of the first data bus, with respect to claim 103, a packet separator able to repack data packets received from the first data bus into a format of the transmission path that is different to the format of the first data bus, with respect to claim 113, an acknowledge code generator that generates an

acknowledgement to be sent to the originator of a data packet accepted from the data bus it is connected to and transmitted via a transmission path to a predetermined destination different to itself, with respect to claim 117, a response packet generator that generates a response to the destination of an acknowledge code.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

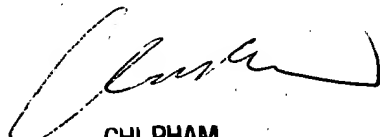
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2616

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones

April 3, 2006



CHI PHAM
SUPERVISORY PATENT EXAMINER
ELECTRONIC BUSINESS CENTER
4/3/06